AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

1. (Original) A system for aligning a wafer to a reticle, comprising:

the reticle, including:

a design area;

a first alignment mark; and

a second alignment mark which is symmetric to the first alignment mark with respect to a reticle centerpoint;

at least one additional diagonal line intersecting at least one alignment mark utilized to facilitate a more accurate alignment of components and wires in accordance with the X initiative

2. (Original) The system of claim 1, further comprising a processor which allows a user to select and place at least one additional diagonal line to intersect at least one alignment mark.

3. (Original) The system of claim 1, the diagonal line is one of 45, 135, 225 and 315 degrees relative to first and second alignment marks, wherein an alignment mark comprises two lines which intersect and are orthogonal.

4. (Original) The system of claim 1 further comprising a memory operatively coupled to the processor to facilitate adding additional lines based on prior operations.

5. (Original) The system of claim 1, the processor determines the number of additional lines required to achieve a desired accuracy within an alignment mark.

6. (Original) A wafer alignment system employing the system of claim 1.

7. (Original) A wafer fabrication system employing the system of claim 1.

8. (Original) A system for aligning two or more wafer layers, comprising:

a reticle, including:

a design area;

a first overlay target; and

a second overlay target which is symmetric to the first overlay target with respect to a reticle centerpoint;

at least one additional diagonal line segment utilized to facilitate a more accurate overlay; and

a processor which allows a user to select and place at least one additional diagonal line segment.

9. (Original) The system of claim 8 wherein a diagonal line is a line that is at least one of 45, 135, 225 or 315 degrees relative to an alignment mark comprising two lines which intersect and are orthogonal.

10. (Original) The system of claim 8 further comprising a memory operatively coupled to the processor to facilitate adding additional lines based on prior operations.

11. (Original) The system of claim 8 wherein the processor determines the number of additional lines required achieving a desired accuracy within an overlay target.

12. (Original) A wafer overlay alignment system employing the system of claim 7.

13. (Original) A wafer fabrication system employing the system of claim 7.

14 – 19. (Cancelled)

20. (Previously Presented) A method for facilitating wafer alignment comprising the steps of:

using a reticle, including:

a design area:

a first alignment mark;

a second alignment mark which is symmetric to the first alignment mark with respect to a reticle centerpoint; and

adding at least one additional diagonal line intersecting at least one alignment mark utilized to facilitate a more accurate alignment.

21 – 22. (Cancelled)

23. (Original) A method for facilitating wafer alignment, comprising the steps of:

using a reticle, including:

a design area;

a first overlay target; and

a second overlay target which is symmetric to the first overlay target with respect to a reticle centerpoint;

adding at least one additional diagonal line segment utilized to facilitate a more accurate overlay; and

selecting and placing at least one additional diagonal line segment utilizing a processor.

24. (Cancelled)

25. (Original) A method of aligning a wafer and measuring overlay error, the method comprising:

means for adding at least one additional diagonal line to an alignment mark to facilitate more accurate wafer alignment;

means for adding at least one additional diagonal line segment to facilitate a more accurate overlay; and

means for selecting and placing at least one additional diagonal line to intersect at least one alignment mark utilizing a processor.

26. (New) The system of claim 1, further including surface inspection equipment, comprising:

at least one CD-SEM;

a scanning apparatus facilitating the inspection of the surface at at least one of 0, 45, 90, 135, 180, 225, 270, 315 or 360 degrees;

a processor; and

a wafer surface that includes at least one feature.

27. (New) A wafer inspection system employing the system of claim 26.

28. (New) A wafer fabrication system employing the system of 26.

29. (New) The system of claim 26, the surface is comprised of a semiconductor material.

30. (New) The system of claim 26, the processor utilized to determine a best angle or angles to inspect a surface feature.

31. (New) The system of claim 26, further comprising a receiving element operatively coupled to the CD-SEM.

32. (New) The method of claim 20, further comprising selecting and placing at least one additional diagonal line to intersect at least one alignment mark utilizing a processor.

33. (New) The method of claim 32 wherein the diagonal line comprises at least one of 0, 45, 90, 135, 180, 225, 270, 315 and 360 degrees relative to the alignment mark.

34. (New) The method of claim 23, facilitating surface inspection utilizing surface inspection equipment, comprising:

employing at least one CD-SEM;

locating surface features to be measured;

scanning the inspection surface at at least one of 0, 45, 90, 135, 180, 225, 270, 315 or 360 degrees; and

processing information to determine a best angle or angles to inspect a surface feature.